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Electric and Electronic Components in Motor Vehicles - 48V On-Board Electrical System Requirements and Test Conditions

Foreword

This edition of this Standard is based on the document LV 148 which has been established by representatives of the automotive manufacturers AUDI AG, BMW AG, Daimler AG, Porsche AG and Volkswagen Aktiengesellschaft within Working Group AK 4.14, AG1 "14V On-Board Electrical System".
If in individual cases modifications to individual test sections are required, such modifications shall be agreed separately between the departments responsible of the automotive manufacturer and the supplier.
Within the framework of common development projects of the automotive manufacturers, test reports will be recognized provided that the tests have been performed by an independent institute accredited in accordance with DIN EN ISO/IEC 17025. Approval does not automatically follow from acceptance of the test reports. Other test reports may be recognized at the discretion of the customer.

The contents of LV 148 edition 2013-07 have been adopted unchanged into the set of standards of Mercedes-Benz. AK-LV documents cited in this MBN LV are usually adopted into the set of Mercedes-Benz standards as MBN LV documents with identical number.

Application note:
Application of the present version of this Standard is binding for new vehicle projects or components of this scope, for which no concept/basic specifications or component requirement specifications have been approved yet at the date of issue of this version.
The respective contract documents regulate the mandatory application of the present version of this Standard by the supplier.

General requirements

For safety requirements, homologation (in particular, exhaust emissions) and quality, the existing statutory requirements and laws shall be complied with. In addition, the relevant requirements of the Daimler Group apply.
All materials, procedures, processes, components, and systems shall conform to the current regulatory (governmental) requirements regarding regulated substances and recyclability.

Changes

In comparison with edition MBN LV 148 2012-03, the following changes have been made: see page 2 of LV 148

NOTE: This translation is for information purposes only.
The German version shall prevail above all others.

Electric and Electronic Components in Motor Vehicles

48-V Electric System

Requirements and Tests

Preface

This Supply Specification (LV) in the present issue was developed by representatives of automobile manufacturers Audi AG, BMW AG, Daimler AG, Porsche AG, and Volkswagen AG in working group (AK) 4.14, team (AG) 1, "14-V/48-V electric system and electric energy management."

This LV is stored as an MS Word file in the Audi AG Standards department.

No claim is made as to its completeness. The automobile manufacturers are entitled to require additional tests corresponding to the relevant state-of-the-art at any time.

Since the individual automobile manufacturers may make changes if necessary, only the automobile manufacturers' in-house standards that are based on this LV must be used.

Deviations from this LV are listed in the in-house standards on the cover sheet (in justified exceptional cases, deviations can be presented in italics in the text of the standard). If modifications of individual test sections are required in individual cases, these modifications must be agreed upon separately between the appropriate departments of the automobile manufacturer and of the supplier.

For general development projects of the automobile manufacturers, test reports will be accepted as long as the tests were performed by an independent institute that is accredited as per DIN EN ISO/IEC 17025. Acceptance of the test reports does not automatically result in a release. Other test reports may be accepted at the discretion of the purchaser.

Dates of versions and revision record

Date	Section	Brief description	Responsible
2011-08-29	All	New issue	Mr. Radon (on behalf of AK 4.14, AG 1)
2013-07-18	2.1	Revised/updated	Mr. Radon (on behalf of AK 4.14, AG 1)
	2.3.2	Fig. 1 revised/updated	
	2.3.2	Storage protection voltage range updated	
	2.3.3	Revised/updated	
	2.5	Revised/updated	
	3.1.1	Revised/updated	
	3.1.2	Tab. 7 revised/updated	
	3.1.2	Fig. 3 added	
	3.1.3	Revised/updated	
	3.2	E48-01b Overvoltage in …	
	3.2.1	Revised/updated	
	3.2.2	Fig. 4 revised/updated	
	3.2.2	Tab. 8 revised/updated	
	3.3	E48-02 Transient overvoltage	
	3.3.1	Revised/updated	
	3.3.2	Fig. 5 revised/updated	
	3.4.2	Fig. 6 revised/updated	
	3.5.2	Fig. 7 revised/updated	
	3.5.2	Tab. 11 corrected; $V_{48max\underline{min},unlimited}$	
	3.6.2	Tab. 12 revised/updated	
	3.6.3	Tab. 13 revised/updated	
	3.6.3	Fig. 8 revised/updated	
	3.7.1.2	Fig. 9 revised/updated	
	3.7.1.2	Tab. 14 revised/updated	
	3.7.2.2	Fig. 10 revised/updated	
	3.7.3.2	Fig. 11 revised/updated	
	3.7.4	Revised/updated	
	3.8.2	Fig. 12 revised/updated	
	3.9.2	Tab. 18 revised/updated	
	3.9.2	Fig. 13 revised/updated	
	3.10.2	Fig. 14 revised/updated	
	3.11.2	Tab. 20 revised/updated	
	3.11.2	Fig. 16 revised/updated	
	3.11.3.2	Revised/updated	
	3.12.2	Revised/updated	
	3.12.2	Fig. 17 revised/updated	
	3.13.2	Fig. 18 revised/updated	
	3.14.2	Tab. 23 revised/updated	
	3.14.2	Fig. 19 revised/updated	
	3.14.3	Revised/updated	
	3.16.2	Tab. 25 "In B1" deleted	
	3.16.2	Fig. 20 revised/updated	
	3.17.2	Tab. 26 "In B1" deleted	
	3.17.2	Fig. 21 revised/updated	
	3.18.2	Tab. 27 "In B1" deleted	
	3.18.2	Fig. 22 revised/updated	
	3.19.1	Fig. 23 revised/updated	
	3.20.2	Fig. 24 revised/updated	
	3.23 (new)	Test E48-21 added	
	4	Tab. 33 revised/updated	

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Scope

This document specifies requirements, test conditions, and tests for electric, electronic, and mechatronic components and systems for the use in motor vehicles.

Additional or deviating requirements, test conditions, and tests must be defined in the pertinent Component Performance Specifications.

The described tests are not used for component qualification or a qualification of the manufacturing process.

Part I – Electrical requirements[1]

1 Referenced standards

The following cited documents, see Table 1, are required for the use of this document. For dated references, only the referenced issue is valid. For undated references, the most recent issue of the referenced document (including all changes) is valid.

Table 1: Referenced standards

DIN 72552-2	Terminal Markings for Vehicles; Codes
DIN 72552-4	Terminal Markings for Vehicles; Summary
DIN EN ISO/IEC 17025	General Requirements for the Competence of Testing and Calibration Laboratories
ISO 6469-3	Electrically Propelled Road Vehicles – Safety Specifications – Part 3: Protection of Persons Against Electric Shock
ECE-R100	Uniform Provisions Concerning the Approval of Battery Electric Vehicles with Regard to Specific Requirements for Design and Functional Safety
LV 124	Electric and Electronic Components in Motor Vehicles up to 3,5 t – General Component Requirements, Test Conditions, and Tests

[1] Part IIff.: See LV 124

2 General part

- LV 148 is an amendment to LV 124. It comprises the additional electrical tests of the 48 V electric system (BN48).
- LV 148 is valid for all components used in the 48-V electric system.

2.1 Premises for components with BN48 connection

- For DC voltage ≤ 60 V, no electrical shock protection is required. This applies to DC voltages up to an electric system ripple of max. 10% RMS value.
  For AC voltage V_{eff} ≤ 30 V, no electrical shock protection is required (ISO 6469-3).
- A single fault in the wiring harness must not cause the BN48 to short circuit to the 12-V electric system (BN12)/24-V electric system (BN24) areas.
- There is a shared ground for BN12/BN24 and BN48, which are connected by spatially separated ground bolts/connections.
- All voltage and current specifications refer to the component (terminal voltage).
- Reversed polarity of the BN48 system is precluded by suitable solutions in the vehicle.
- An external start of BN48 is precluded by suitable solutions in the vehicle.

2.2 Requirements for components with BN48 connection

- A single fault must not cause the BN48 to short circuit to the BN12/BN24.
- Components with parallel BN48 supply and BN12/BN24 supply, or connection between BN12 and BN48, require individual ground connections for both supply areas. These ground connections must be spatially separated from each other.
- The loss of ground connection of a BN48 component (T.31 and/or T.41) must not cause communication networks and electrical networks to malfunction or be destroyed.
- No component must enter the overvoltage range (e.g., due to a load dump or resonance step-up.
- Overcurrent tests must be specified in the Component Performance Specifications.

2.3 Terms and definitions

2.3.1 Terminal designations

Terminal 40 is the positive line of the 48 V supply.
Terminal 41 is the ground cable of the 48 V supply.
The terminal designation is stipulated in DIN 72552-2 and DIN 72552-4.

2.3.2 Voltages and currents

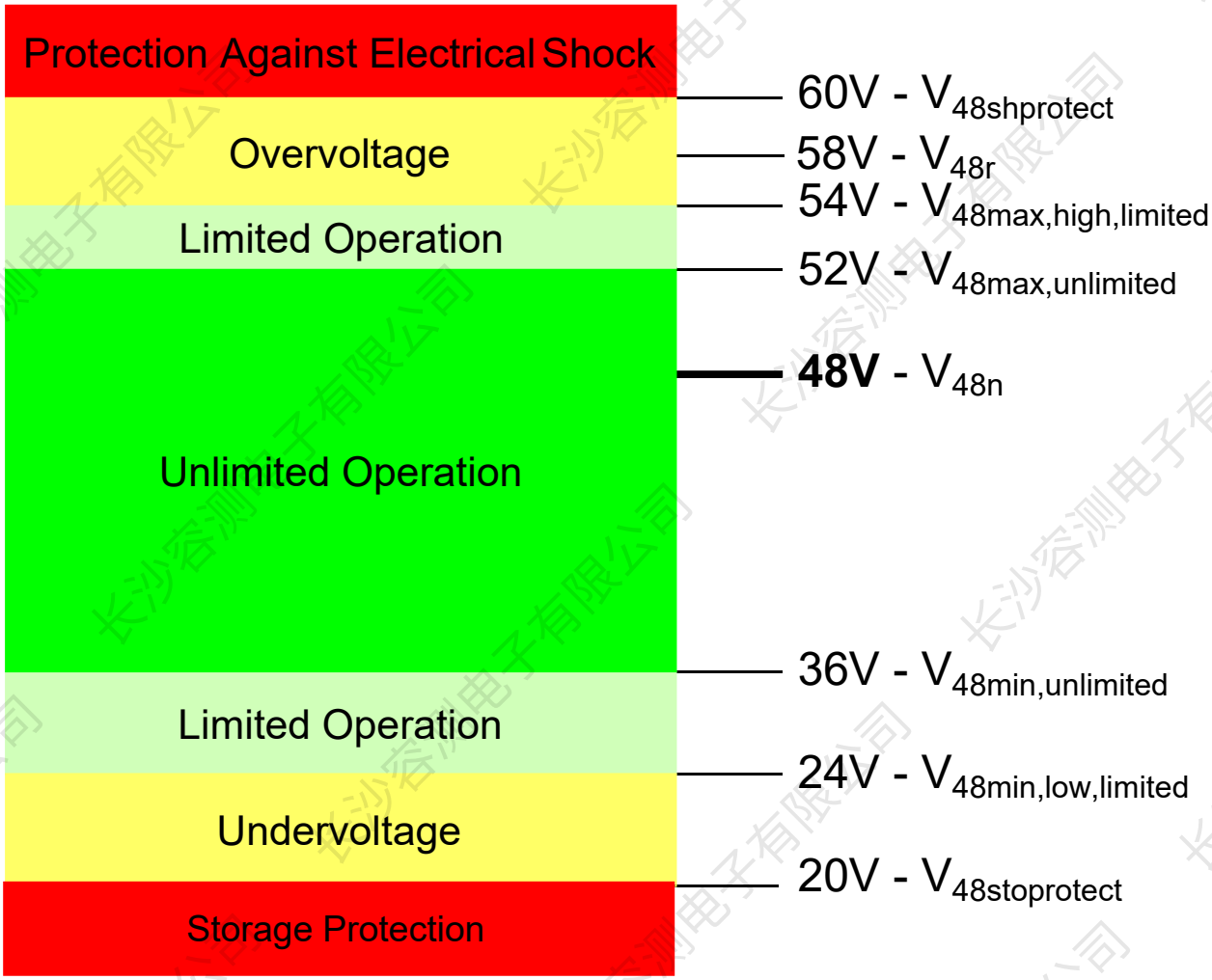

Figure 1: Definitions of the static voltage ranges

Electrical shock protection range

In this range, DC voltages require electrical shock protection (see ECE-R 100).

Overvoltage range

The overvoltage range including all tolerances is between $V_{48max,high,limited}$ and V_{48r}. In this range, the overvoltage protection must be active and voltages higher than $V_{48max,high,limited}$ must be recorded by an event memory entry.

The range between V_{48r} and $V_{48shprotect}$ includes the safety margin.

Upper operating voltage range with functional limitation

The range between $V_{48max,unlimited}$ and $V_{48max,high,limited}$ is used for calibrating the storage and the accommodation of backfeed energy.

Operating voltage range without functional limitation

The range between $V_{48min,unlimited}$ and $V_{48max,unlimited}$ allows the components to be operated without functional limitation.

Lower operating voltage range with functional limitation

Operation within the range from $V_{48min,low,limited}$ to $V_{48min,unlimited}$ is only temporarily permissible.

Remedial action to return to the operating voltage range without functional limitation is required.

Undervoltage range

All voltages below $V_{48min,low,limited}$ are defined as undervoltage and must be recorded as an event memory entry. The storage protection voltage is at $V_{48stoprotect}$.

Storage protection voltage range

All voltages below $V_{48stoprotect}$.

Table 2: Abbreviations for voltages and currents

Abbreviation	Description	Value
$V_{48shprotect}$	Electrical shock protection voltage. Derived from the requirement to adhere to the limit value for electrical shock protection for DC voltages (see ECE-R 100)	60 V
V_{48r}	2 V safety margin to the electrical shock protection voltage	58 V
$V_{48max,high,limited}$	Maximum voltage of the upper operating range with functional limitation	54 V
$V_{48max,unlimited}$	Maximum voltage of the operating range without functional limitation	52 V
V_{48n}	BN48 nominal voltage	48 V
$V_{48min,unlimited}$	Minimum voltage of the operating range without functional limitation	36 V
$V_{48min,low,limited}$	Minimum voltage of the lower operating range with functional limitation	24 V
$V_{48stoprotect}$	Storage protection voltage	20 V
V_{48pp}	Peak-to-peak voltage	
V_{48rms}	RMS value of a voltage	
V_{48max}	Maximum voltage that may occur during a test	
V_{48min}	Minimum voltage that may occur during a test	
V_{48test}	BN48 test voltage	
V_{12test}	BN12 test voltage	
GND48	Device ground (T.41)	

2.3.3 Test setup

The general conditions from DIN EN ISO/IEC 17025 apply.

Unless explicitly stated otherwise, the specified voltage curves refer to the terminal voltages of the device under test (DUT). They must be measured using the test setup and documented.

The specified voltage thresholds under $V_{48shprotect}$ must be adhered to on the component with an accuracy
of ±1% (measured at the connector or at the control module terminal).

A tolerance margin of 0% to -1% applies to the $V_{48shprotect}$ threshold.

Before each test the event memory must be cleared.

After each test the event memory must be read and documented.

All BN48 components with an interface to the BN12 supply or with communication interfaces must additionally fulfill LV 124:

- BN12 must fulfill the requirements of LV 124. During the tests as per LV 124, the voltage is V_{48n} unless specified otherwise in the individual tests of LV 124.
- During the tests of BN48, the BN12 voltage is 14,0 V unless specified otherwise in the individual tests.

It must be ensured in addition, and documented accordingly, that a random voltage or a random voltage curve within the defined limits on BN48 does not destroy the component on BN12 or cause a function failure. This also applies to destruction of the DUT due to the test pulse on the BN48 side.

See Figure 2: Component with two voltage supplies.

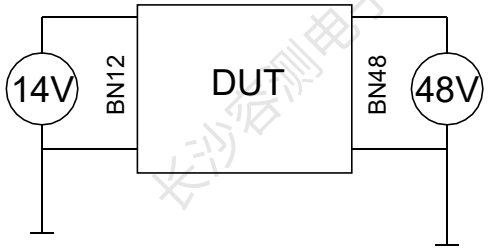

Figure 2: Component with two voltage supplies

2.3.4 Temperatures

Table 3: Abbreviations for temperatures

Abbreviation	Description	Unit
T_{min}	Minimum operating temperature	°C
T_{RT}	Room temperature	°C
T_{max}	Maximum operating temperature	°C
T_{test}	Test temperature	°C

2.3.5 Times

Table 4: Abbreviations for times

Abbreviation	Description	Unit
t_r	Rise time, e.g., of a voltage curve	ms
t_f	Fall time, e.g., of a voltage curve	ms
t_{test}	Test duration	s, min, h

All edge descriptions refer to the 10% or 90% voltage values.

2.3.6 Standard tolerances

Unless otherwise indicated, the tolerances as per Table 5: Definition of standard tolerances apply.

Tolerances of envelopes must always be considered unilaterally as, otherwise, the requirement is mitigated.

Tolerances refer to the required set value.

Table 5: Definition of standard tolerances

Abbreviation	Description	Tolerance limits
f	Frequencies	±1%
T	Temperatures	±2 °C
H_{rel}	Relative humidity	±5%
t	Times	+5% to 0%
V	Voltages	±0,5%
I	Currents	±2%

2.3.7 Standard values

Unless otherwise indicated, the standard values as per Table 6: Definition of standard values apply.

Table 6: Definition of standard values

Abbreviation	Description	Value
T_{RT}	Room temperature	23 °C ±5 °C
H_{rel}	Relative humidity	25% (+5% to 0%) to 75% (-5% to 0%)
T_{test}	Test temperature	T_{RT}
R_i	Internal resistance of the voltage source	10 mΩ ≤ R_i ≤ 100 mΩ

2.4 Sampling rates and measured value resolutions

The sampling rate and bandwidth of the measuring system must be adapted to the respective test. All measured values with all maximum values (peaks) must be recorded.

The resolution of the measured values must be adapted to the respective test. It must be ensured that occurring voltage peaks do not lead to an overflow or cannot be measured in the case of an insufficient resolution.

2.5 Functional statuses

This section describes the functional status of the DUT during and after the test. The functional status of the DUT must be specified for each test. Both the exact functional requirements placed on the DUT in the operating statuses and additional requirements must be defined in the Component Performance Specification and documented.

The functional status A is the highest requirement placed on the component.

The data memory function must be ensured for the duration of storing in all functional statuses.

The integrity (not up-to-dateness) of the non-volatile memories must be ensured at any time.

The functional statuses are entered in the test descriptions in the pertinent figures, using the letters A to D.

2.5.1 Functional status A

The components are operational without limitation and provide their specified function.

2.5.2 Functional status B

The components continue to be operational without limitation. The components provide a function within the deviations permissible for functional status B. The components must automatically provide their specified function on return to functional status A.

2.5.3 Functional status C

The components continue to be operational, must not assume undefined statuses and, in particular, must not cause any other components to malfunction. The components may reduce their electrical power for reasons of self-protection. The components must automatically provide their specified function on return to functional status A or B.

2.5.4 Functional status D

The components continue to be operational, and they must not assume undefined statuses. The components may reduce their electrical power to zero. At the end of the exposure, the DUT must return to functional status A by means of a reset (e.g., change of ignition status, new start of the vehicle).

2.6 Operating modes

The electric, electronic, and mechatronic components and systems are operated in different operating modes during service life, which must be simulated correspondingly during the tests. Details concerning the operating modes, operating loads (e.g. triggering, original sensors, original actuators or replacement circuitry) and the required preconditions must be agreed upon between contractor and purchaser and must be documented.

The operating mode required during the test must represent the most demanding requirement for the component. Deviations must be defined in the Component Performance Specification.

2.6.1 Operating mode I – DUT not electrically connected

2.6.1.1 Operating mode I.a

The DUT is without current, connectors and wiring harness are not connected.

2.6.1.2 Operating mode I.b

The DUT is without current, but connectors and wiring harness are connected.

2.6.2 Operating mode II – DUT electrically connected

Components that are electrical source and sink must be tested in both operating modes.

2.6.2.1 Operating mode II.a

The DUT must be operated without operating load.

2.6.2.2 Operating mode II.b

The DUT must be operated with minimal operating load.

The DUT must be operated in a way that minimal self-heating occurs (e.g., by reducing a continuous output power or by infrequent activation of external loads).

2.6.2.3 Operating mode II.c

The DUT must be operated with maximum operating load.

The DUT must be operated in a way that maximum self-heating occurs (e.g., by means of a realistic maximization of a continuous output performance or frequent activation of external loads).

2.7 Parameter test

All parameters that must be separately monitored during the test must be defined in the Component Performance Specification for the pertinent tests with value ranges.

2.8 Continuous parameter monitoring with drift analysis

The key parameters to be monitored must be recorded during the whole test.

For components with event memory, the event memory must be monitored continuously and the entries must be documented.

The data resulting from the continuous parameter monitoring must be examined for trends and drifting to detect irregularities, aging, or malfunctions of the component.

2.9 Physical analysis

For the physical analysis, the DUT must be opened and visually inspected for damage.

Additional analyses (e.g. X-ray examinations and metallographic examinations of the assembly and joining technology) must be coordinated between purchaser and contractor.

2.10 Interface description

All interfaces must be described completely in their statuses and electrical properties. This description serves as a basis for the evaluation of the test results and, thus, must be available in detail.

3 Electrical requirements and tests

Each DUT systematically goes through all tests.

After each individual test, the DUT is checked for external integrity and tested for unlimited functionality before the next test is performed. The test for unlimited functionality must be defined in the Component Performance Specification.

Damaged DUTs must be withdrawn from the test cycle and documented. If applicable, the test must be repeated with a new DUT, or the following test must be performed with a new DUT. The procedure must be agreed upon with the purchaser.

The test plan must be agreed upon with the purchaser.

The functional status specified in the test is the minimum requirement for this test.

The permissible event memory entries and the functional statuses of the component must be specified for each test.

3.1 E48-01a Long-term overvoltage

3.1.1 Aim

The component's resistance to long-term overvoltage is tested.

3.1.2 Test

Table 7: Test parameters E48-01a Long-term overvoltage

DUT operating mode	Operating mode II.a, II.b, and II.c
t_0	Functional status A assumed
t_r	0,1 s
t_{test}	60 min
V_{48test}	$V_{48shprotect}$
T_{test}	T_{max} -20 °C
Number of cycles	1
Number of DUTs	6

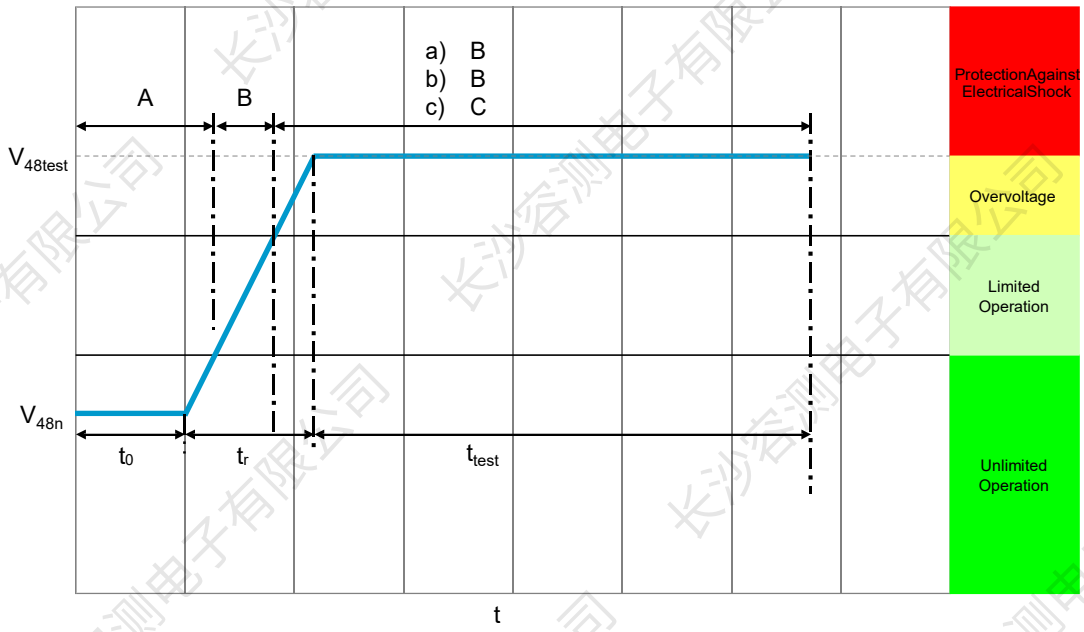

Figure 3: Test pulse E48-01a Long-term overvoltage

3.1.3 Requirement

The evaluation of the test results depends on the use of the component. A distinction is made between:

a) Components that are designed
to handle high levels of electrical power (e.g., ohmic loads): Functional status B
b) Functions required for driving operation: Functional status B
c) For all other components: Functional status C

3.2 E48-01b Overvoltage in backfeeding components

3.2.1 Aim

This test applies for all backfeeding components because they must have a voltage-limiting function to ensure protection against electrical shock. A scenario is simulated in which the component feeds power to the BN48 which cannot be accommodated by the electric system, therefore causing a voltage increase.

3.2.2 Test

The DUT is connected to a powerful source.

During operating mode II.c with maximum backfeed, the source must be immediately separated from the component.

Table 8: Test parameters E48-01b Overvoltage in backfeeding components

DUT operating mode	Operating mode II.c
T_{test}	T_{RT}
V_1	$V_{48max,unlimited}$
V_2	V_{48r}
V_3	$V_{48max,high,limited}$
t_0	After reaching the maximum backfeed output
t_1	After falling below V_3
Number of cycles	3
Number of DUTs	6

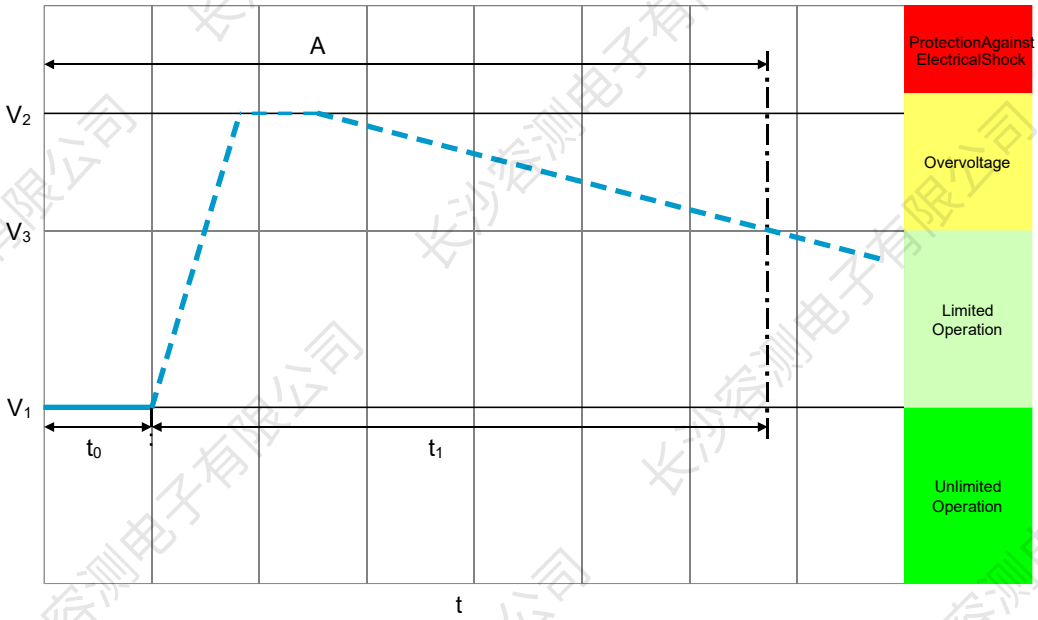

Figure 4: Test pulse E48-01b Overvoltage in backfeeding components

3.2.3 Requirements

Functional status A

The voltage on the component must be ≤V_{48r} during the entire test.

3.3 E48-02 transient overvoltage

3.3.1 Aim

Transient overvoltages may occur in the BN48. These overvoltages are simulated by means of this test.

3.3.2 Test

Table 9: Test parameters E48-02 Transient overvoltage

DUT operating mode	Operating mode II.c
V_0	V_{48n}
V_1	70 V
V_2	V_{48r}
t_0	100 ms
t_r	1 ms
t_1	100 ms
t_f	1 ms
t_2	600 ms
t_{3a}	2,5 s
t_{3b}	9 s
R_i	10 mΩ ≤ R_i ≤ 100 mΩ
Number of cycles	1. Short test: 3x with t_{3a} 2. Long test: 1 000x with t_{3b} Both tests are carried out in succession.
Number of DUTs	6

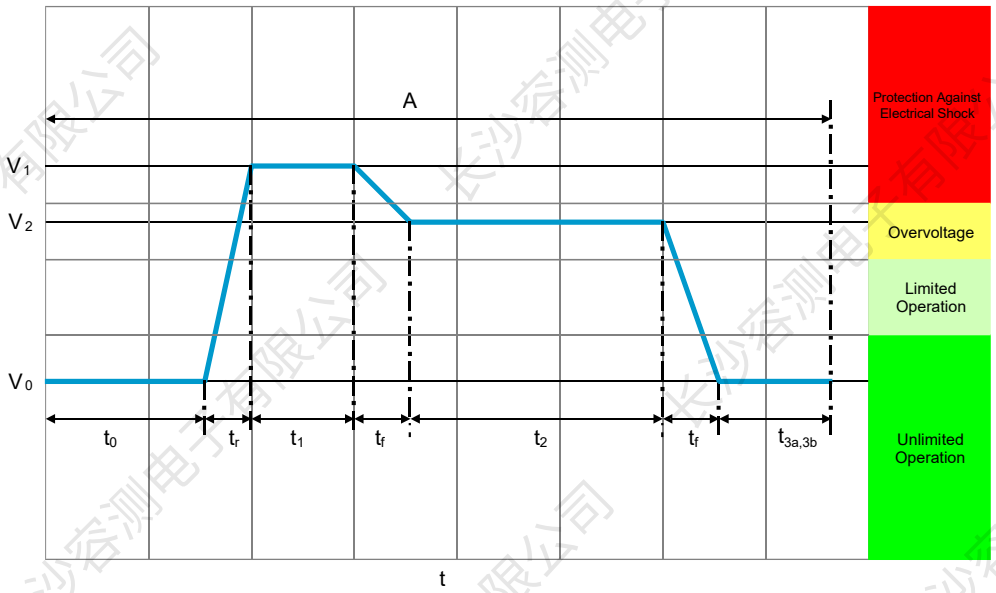

Figure 5: Test pulse E48-02 Transient overvoltage

3.3.3 Requirements

Functional status A

3.4 E48-03 Transient process in the lower operating range with limited function

3.4.1 Aim

Transient undervoltages in the electric system may occur due to switching on of loads. These undervoltages are simulated by means of this test.

3.4.2 Test

Table 10: Test parameters E48-03 Transient process in the lower range with limitations

DUT operating mode	Operating mode II.c
V_0	$V_{48min,unlimited}$
V_1	$V_{48min,low,limited}$
t_0	60 s
t_f	1,8 ms
t_1	500 ms
t_r	1,8 ms
t_2	500 ms
Number of cycles	1
Number of DUTs	6

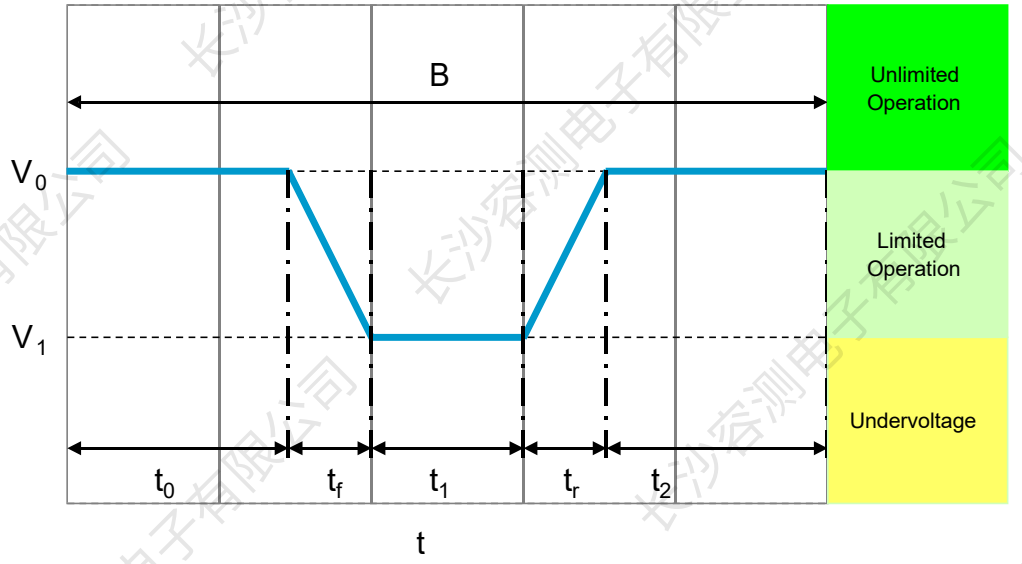

Figure 6: Test pulse E48-03 Transient process in the lower range with limitations

3.4.3 Requirement

Functional status B

3.5 E48-04 Recuperation

3.5.1 Aim

This test simulates a longer phase of recuperation.

3.5.2 Test

Table 11: Test parameters E48-04 Recuperation

DUT operating mode	Operating mode II.c
V_0	$V_{48max,unlimited}$
V_1	$V_{48max,high,limited}$
t_0	60 s
t_r	100 ms
t_1	60 s
t_f	100 ms
t_2	60 s
Number of cycles	1
Number of DUTs	6

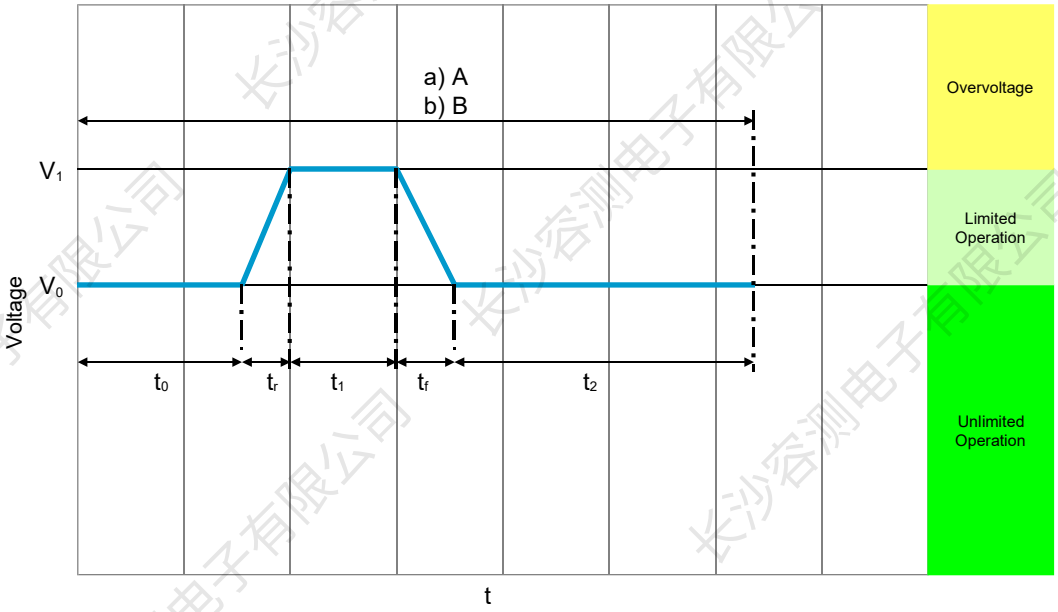

Figure 7: Test pulse E48-04 Recuperation

3.5.3 Requirements

The evaluation of the test results depends on the use of the component. A distinction is made between:

a) Components relevant for recuperation and driving operation: Functional status A
b) For all other components: Functional status B

3.6 E48-05 Superimposed AC voltage

3.6.1 Aim

Voltages may be superimposed to the electric system. The superimposed AC voltage may be applied during the entire generator operation mode. This situation is simulated by means of this test.

3.6.2 Test part 1

Table 12: Test parameters E48-05 Superimposed AC voltage

DUT operating mode	Operating mode II.c
R_i	R_i = 60 mΩ
V_{48test}	$V_{48min,unlimited}$
t_{test}	30 min
f	F1: 15 Hz to 30 kHz F2: 30 kHz to 200 kHz
Wobble period	2 min
Wobble type	Triangle, logarithmic
V_{48pp}	For F1: 6 V (to be set before DUT is connected) For F2: 2 V (to be set before DUT is connected)
Number of DUTs	6

3.6.3 Test part 2

Table 13: Test parameters E48-05 Superimposed AC voltage

DUT operating mode	Operating mode II.c
R_i	R_i = 60 mΩ
V_{48test}	$V_{48max,unlimited}$
t_{test}	30 min
f	F1: 15 Hz to 30 kHz F2: 30 kHz to 200 kHz
Wobble period	2 min
Wobble type	Triangle, logarithmic
V_{48pp}	For F1: 6 V (to be set before DUT is connected) For F2: 2 V (to be set before DUT is connected)
Number of DUTs	6

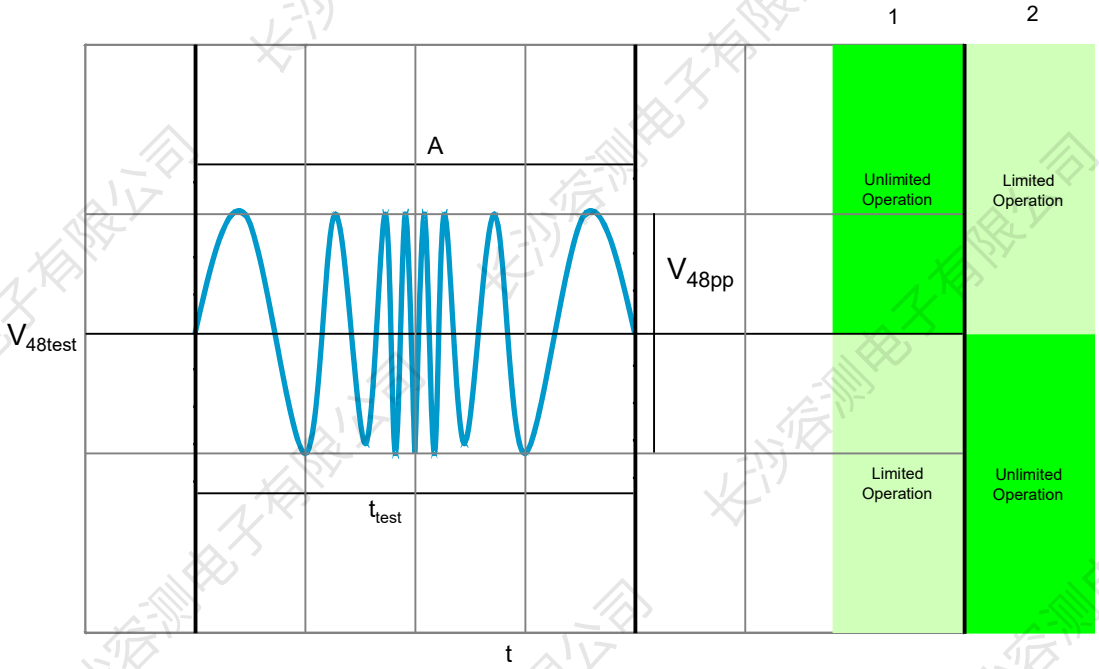

Figure 8: Test pulse E48-05 Superimposed AC voltage

3.6.4 Requirements for parts 1 and 2

Functional status A

All outputs must remain within the defined limits during the test. This must be verified during the complete test duration.

3.7 E48-06 Slow decrease and increase of the supply voltage

3.7.1 E48-06 for operation without storage

3.7.1.1 Aim

The slow decrease and increase of the supply voltage is examined as it occurs during the slow discharging and charging procedure.

3.7.1.2 Test

Table 14: Test parameters E48-06 Slow decrease and increase of the supply voltage

DUT operating mode	At the beginning of the test, the DUT is in functional status A.
V_0	$V_{48max,unlimited}$
Voltage gradient	±2 V/min
V_1	$V_{48min,unlimited}$
V_2	0 V
t_1	Until the event memory is completely read.
Number of cycles	1 cycle in operating mode II.c 1 cycle in operating mode II.a
Number of DUTs	6

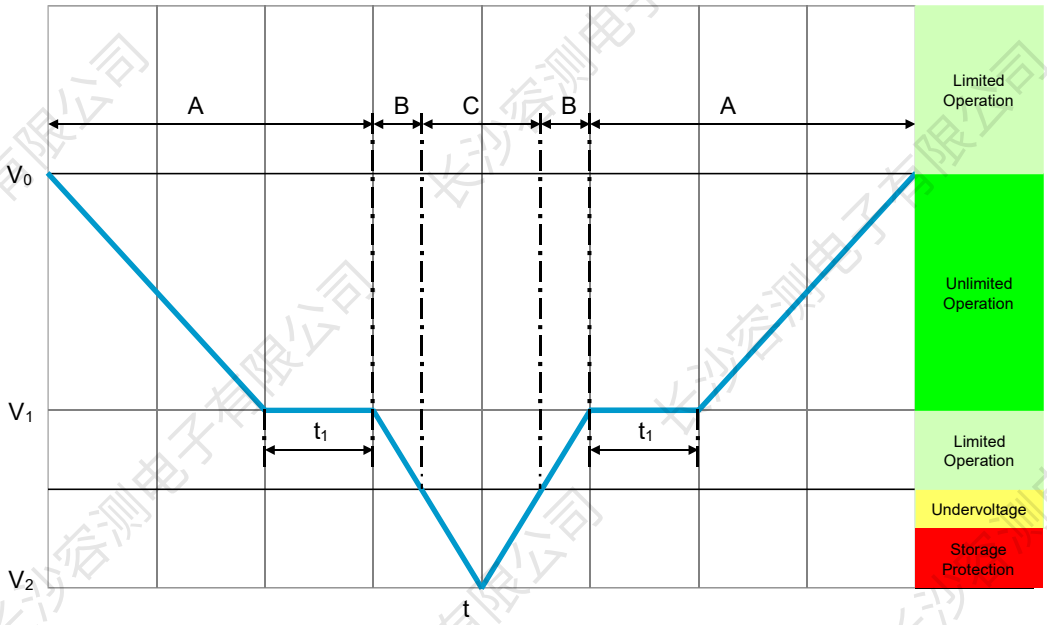

Figure 9: Test pulse E48-06 Slow decrease and increase of the supply voltage

3.7.2 E48-06 for operation with storage, part 1

3.7.2.1 Aim

The slow switch-off of the supply voltage is examined as it occurs after the storage is disconnected.

3.7.2.2 Test

Table 15: Test parameters E48-06 for operation with storage, part 1

DUT operating mode	Operating mode II.a
V_0	$V_{48max,unlimited}$
V_1	$V_{48min,unlimited}$
V_2	$V_{48stoprotect}$
V_3	0 V
t_0	100 ms
t_{f1}	8 min
t_1	≥ 60 s (the event memory is read during this phase)
t_{f2}	8 min
t_2	60 s
t_{f3}	3 s
t_3	60 s
Number of cycles	1 cycle
Number of DUTs	6

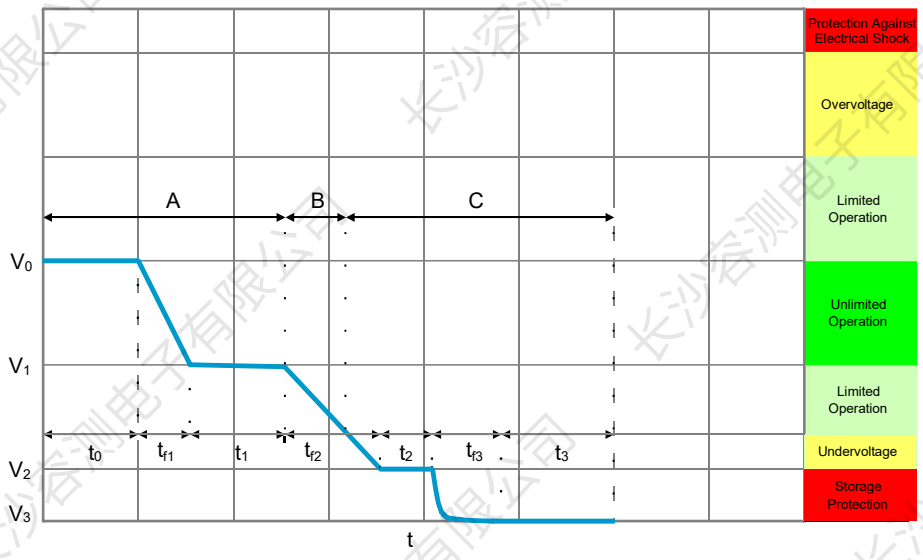

Figure 10: Test pulse E48-06 for operation with storage, part 1

Slow decrease of the supply voltage with storage switch-off

3.7.3 E48-06 for operation with storage, part 2

3.7.3.1 Aim

The connecting of the generator during disconnected storage with subsequent connecting of the discharged storage is examined.

3.7.3.2 Test

Table 16: Test parameters E48-06 for operation with storage, part 2

DUT operating mode	Operating mode II.b after reaching the final voltage
V_0	0 V
V_1	V_{48n}
V_{48pp}	6 V at 10 kHz
V_2	$V_{48stoprotect}$
t_0	100 ms
t_{r1}	300 ms
t_1	≥ 60 s (the event memory is read during this phase)
t_{f1}	1 ms
t_{r2}	14 min
t_3	100 ms
Number of cycles	1 cycle
Number of DUTs	6

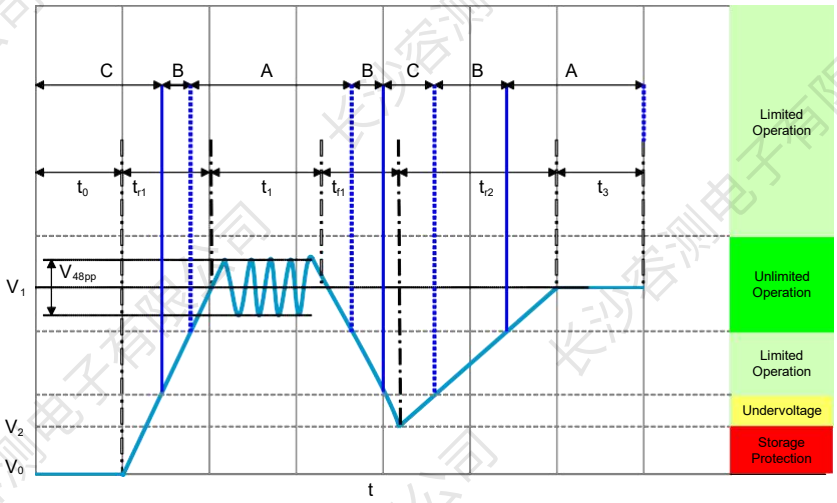

Figure 11: Test pulse E48-06 for operation with storage, part 2

First the generator is connected, followed by the storage.

3.7.4 Requirement

The evaluation of the test results depends on the voltage range that is applied to the component during the test, see Figure 9, Figure 10, and Figure 11.

3.8 E-48-07 Slow decrease, quick increase of the supply voltage

3.8.1 Aim

This test simulates the slow decrease of the electric system voltage to the storage protection voltage with subsequent switch-off to 0 V, followed by the quick reapplication of the storage voltage by a recharged or new storage.

Note: The storage is not activated until it is connected to the electric system (no bouncing during contacting).

3.8.2 Test

Table 17: Test parameters E48-07 Slow decrease and quick increase of the supply voltage

DUT operating mode	Operating mode II.a
V_0	$V_{48max,unlimited}$
V_1	$V_{48min,unlimited}$
V_2	$V_{48stoprotect}$
V_3	0 V
V_4	V_{48n}
t_0	100 ms
t_{f1}	8 min
t_1	≥ 60 s (the event memory is read during this phase)
t_{f2}	8 min
t_2	60 s
t_{f3}	3 s
t_3	300 s
t_{r1}	1 ms
t_4	100 ms
Number of cycles	1 cycle in operating mode II.a
Number of DUTs	6

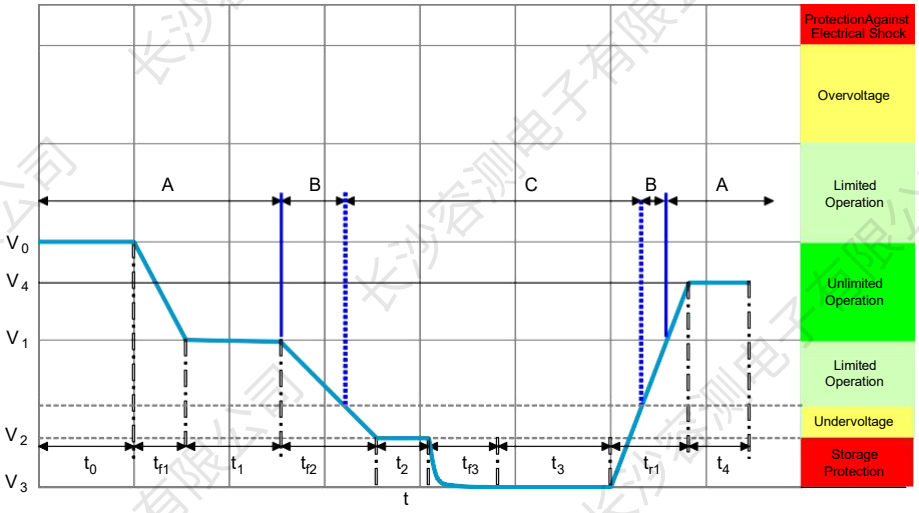

Figure 12: Test pulse E48-07 Slow decrease and quick increase of the supply voltage

3.8.3 Requirement

At the end of the test, the system is in functional status A.

3.9 E48-08 Reset behavior

3.9.1 Aim

The reset behavior of a component is simulated and tested (control unit logic is supplied by BN48) in its environment. Test boundary conditions (e.g. assembly, terminal, system) must be described in detail.

During operation, an arbitrary sequence of repeated switching-on/off procedures occurs; this must not lead to an undefined behavior of the component.

The reset behavior is represented by a voltage variance and a time variance. Two different test sequences are required to simulate different switch-off times. A component must always undergo both sequences.

This test applies only to components with logic supply from BN48.

3.9.2 Test

Table 18: Test parameters, E-48-08 Reset behavior

DUT operating mode	Operating mode II.c
V_0	$V_{48min,unlimited}$
ΔV_1 range between V_0 and V_1	2 V
V_1	$V_{48min,low,limited}$
ΔV_2 (range $V_{48min,low,limited}$ to 0 V)	0,5 V
V_2	0 V
t_0	At least 10 s and until the DUT has returned to 100% operability (all systems rebooted without error).
t_1 – Test sequence 1	5 s
t_1 – Test sequence 2	100 ms
$t_{f/r}$	≤100 ms
Number of cycles	1
Number of DUTs	6

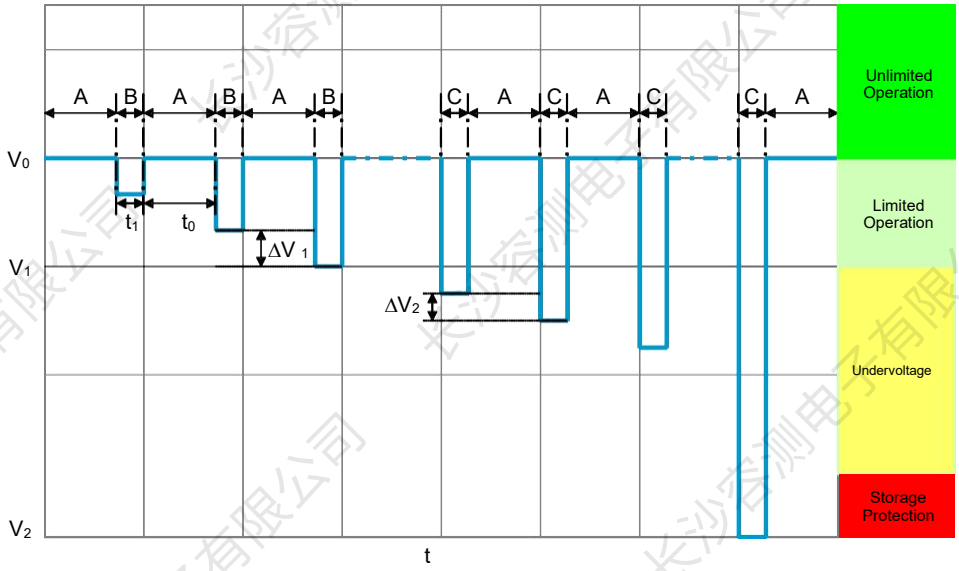

Figure 13: Test pulse E48-08 Reset behavior

3.9.3 Requirement

- Functional status A when $V_{48min,unlimited}$ is reached.
- Functional status B until $V_{48min,low,limited}$
- Functional status C below $V_{48min,low,limited}$

Undefined operating statuses must not occur under any circumstances.

It must be verified and documented that the specified threshold as of which voltage level the component leaves functional status A for the first time is complied with.

3.10 E48-09 Short interruptions

3.10.1 Aim

The component's behavior at short interruptions of different durations is examined.

3.10.2 Test

Table 19: Test parameters E48-09 Short interruptions

DUT operating mode	Operating mode II.c	
Test setup	Schematic circuit as per Figure 15. The artificial network must be agreed upon with the appropriate department. The total resistance R including cable routing is ≤100 mΩ In status "ON," S1 is closed and S2 is open. In status "OFF," S1 is open and S2 is closed.	
V_{48test}	V_{48n}	
t_1	The supply voltage of V_{48test} is interrupted at varying intervals. The following sequence must be complied with for this purpose:	
	100 µs to 1 ms	Steps of 100 µs
	1 ms to 10 ms	Steps of 1 ms
	10 ms to 100 ms	Steps of 10 ms
	100 ms to 2 s	Steps of 100 ms
DUT On – function On	>10 s	
t_2	The test voltage V_{48test} must be maintained at least until the DUT has achieved 100% operability again (all systems rebooted without error).	
Number of cycles	1	
Number of DUTs	6	

The duration of the voltage dip increases at the intervals specified in Table 19. This results in a diagram as shown in Figure 14: Test pulses E48-09 Short interruptions.

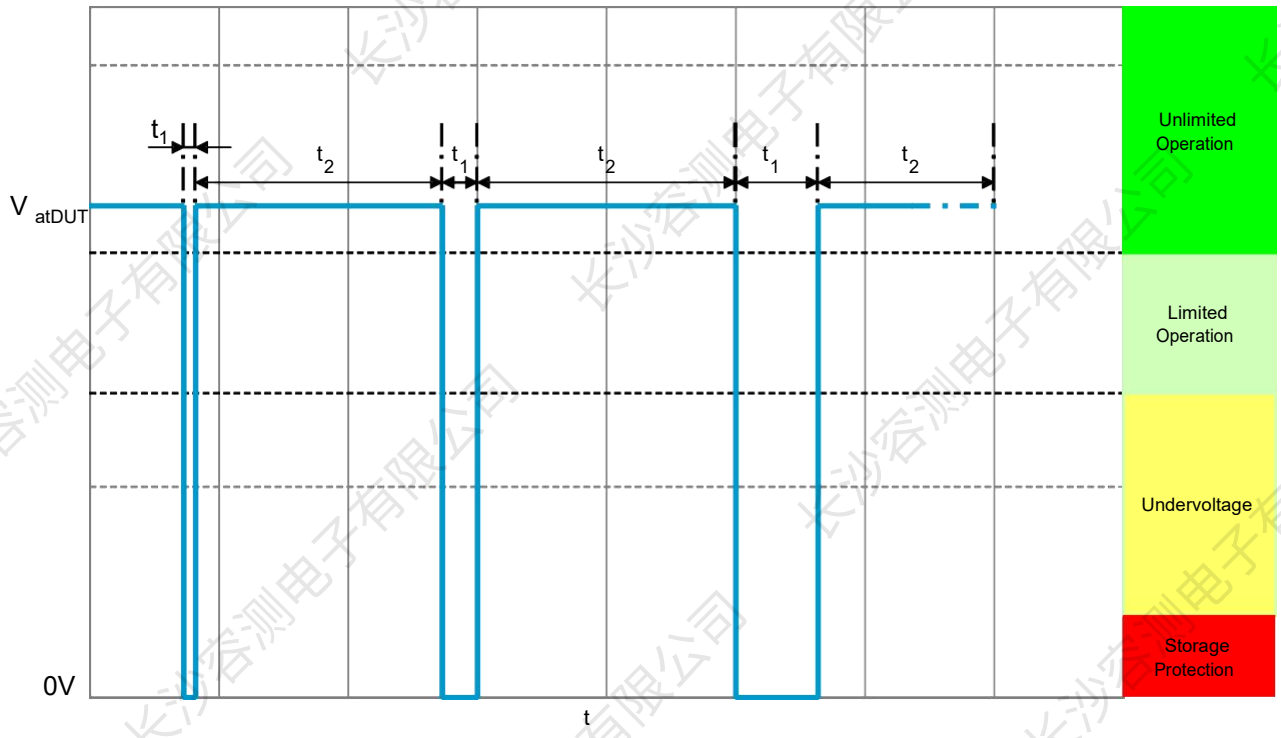

Figure 14: Test pulses E48-09 Short interruptions

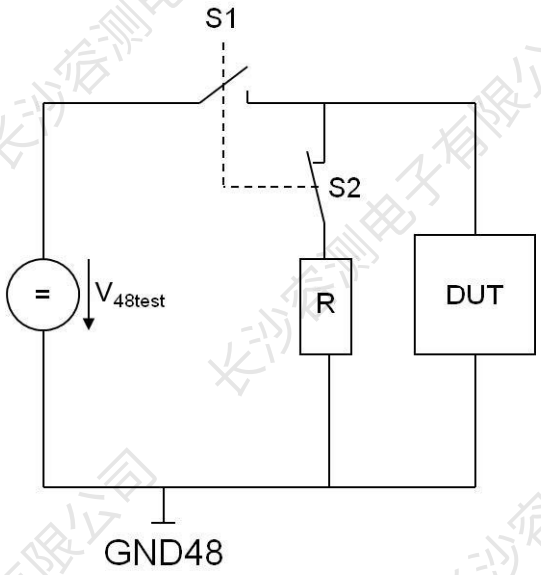

Figure 15: Schematic circuit E48-09 Short interruptions

3.10.3 Requirements

It must be documented as of which time value t_1 the DUT leaves functional status A for the first time.

The test is passed if the DUT achieves functional status A for a time of $t_1 \leq 100$ µs, or otherwise functional status C. A deviating value for the permissibility of functional status C must be defined in the Component Performance Specification.

3.11 E48-10 Start pulses

3.11.1 Aim

When starting the engine, the storage voltage drops to a low value for a short period and then rises again.

3.11.2 Test

Table 20: Test parameters E48-10 Start pulses

DUT operating mode	For components relevant for starting: Operating mode II.c For components not relevant for starting: Operating mode II.b
Test pulse	a) Components relevant for starting Cold start: "normal" and "severe" test pulse b) Components not relevant for starting: Cold start: "normal" test pulse
V_0	V_{48n} for cold start, normal 40 V for cold start, severe
V_1	$V_{48min,low,limited}$
t_0	2 s
t_f	1 ms
t_1	1 s
t_r	1 ms
t_2	2 s
Number of cycles	10
Number of DUTs	6

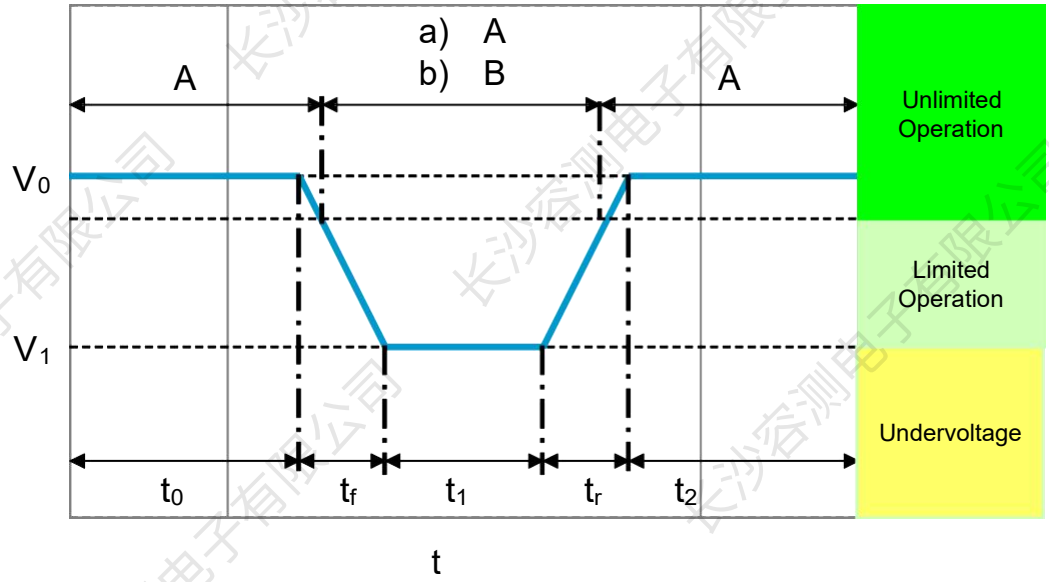

Figure 16: Test pulse E48-10 Start pulses

During hot start, the operating range without functional limitation is not left.

3.11.3 Requirement

3.11.3.1 Components relevant for starting (a)

Event memory entries must not occur.
It must always be possible to start the vehicle.
Test 1 – Cold start
"Normal" test pulse: functional status A
"Severe" test pulse: functional status A

3.11.3.2 Components not relevant for starting (b)

Test 1 – Cold start
"Normal" test pulse: functional status B
"Severe" test pulse: functional status C

3.12 E48-11 Loss of ground BN48

3.12.1 Aim

This test simulates a scenario in which a BN48 component has lost its ground connection. The component is exclusively supplied by the BN48 and has interfaces to BN12 components (e.g., CAN/LIN/FlexRay bus, or other analog or digital signal circuits).

It must be ensured that the loss of ground of the BN48 component does not interfere with the other communication nodes of the BN12 (e.g., due to excessive voltage or reversed polarity). It must also be ensured that the lost ground connection does not destroy any of the components.

3.12.2 General test

- On a test bed, the BN48 device under test (DUT) is connected to the test bed components partial electric system 1 (PES1) and partial electric system 2 (PES2), see Figure 17.
- All signal and bus lines of the DUT are connected to PES1 and PES2:
  - Transmission signals of the DUT are distributed on PES1 and PES2.
  - Reception signals of the DUT are transmitted by PES1.
- PES1 and PES2 simulate the remaining bus and with their interface elements fulfill the requirements from the Component Performance Specification (automotive-qualified and released interface elements).
- Between PES1 and PES2, a bus communication is established that is
  - high performing,
  - bi-directional,
  - secured with message counter and cyclic redundancy check (CRC), and
  - monitored (occurring errors are immediately recognized and recorded).
- The signal circuits between DUT and PES1/2 are
  - monitored in PES1 and PES2 (signal content),
  - and occurring errors are detected in PES1/2 and recorded.
- The voltages and currents of all communication circuits (bus and signal circuits) must be monitored in or on PES1/2 for exceeding the specification limits.

Details must be agreed upon with the owner of the Component Performance Specification.

Table 21: Test parameters E48-11 BN48 loss of ground

DUT operating mode	Operating mode II.c
t_{test}	See tests
V_{48test}	V_{48n}
V_{12test}	14 V
T_{test}	T_{max} -20 °C
Number of cycles in a test	1
Number of DUTs	6

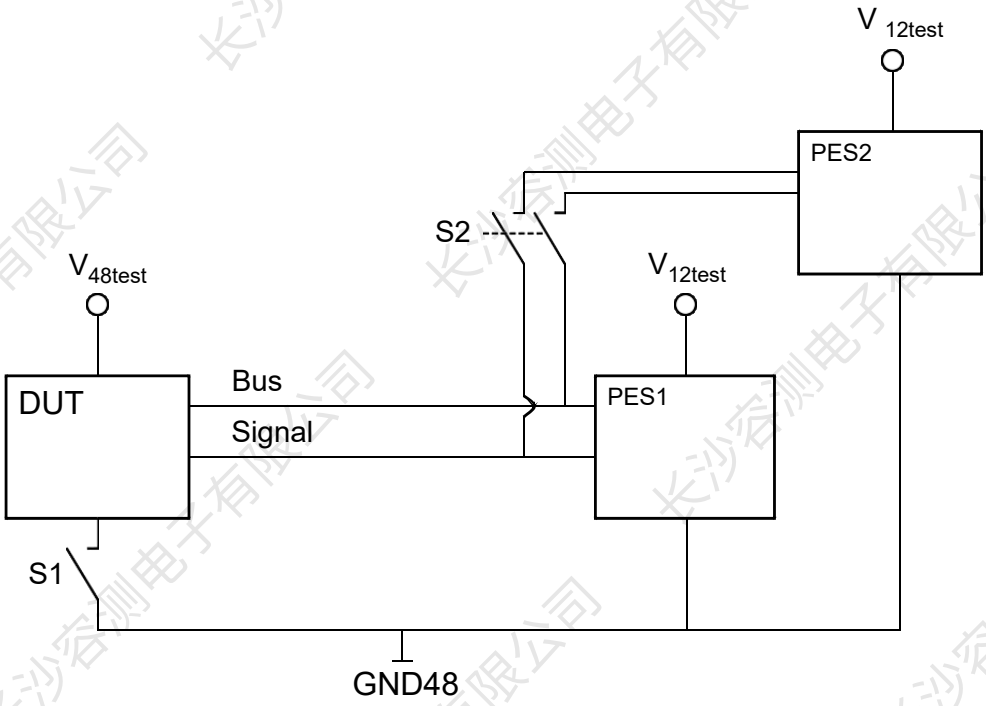

Figure 17: Schematic circuit E48-11 BN48 loss of ground

3.12.3 Test 1

S1 closed
S2 closed
All DUT/PES1/PES2 components work error-free.
S2 is opened.

3.12.4 Requirement 1

Errors in PES1 and PES2 must be recorded:

- PES1: Bus communication with PES2 faulty
- PES2: Bus communication with PES1 faulty
- PES2: Signal circuits faulty

No error in the DUT – functional status A.

3.12.5 Test 2

S1 closed
S2 closed
All DUT/PES1/PES2 components work error-free.
S1 is opened.
The test is continued for 30 min after S1 is opened.

3.12.6 Requirement 2

In PES1 and PES2, no voltages above the defined interface voltages and no currents above the defined interface current must occur. This applies to all bus and signal circuits.

Bus communication: The bus communication between PES1 and PES2 works error-free – no error in the event memory.

Signal circuit:

Distinction of cases

a) DUT reads in this circuit, i.e., PES1 is the sender
   Requirement: No event memory entry in PES1 and PES2
b) DUT is the sender.
   Requirement: Event memory entry in PES1 and PES2 due to loss of signal

3.13 E48-12 Ground offset

3.13.1 Aim

In components with several subsystems, potential differences between the individual supply inputs may occur. It must be ensured that the functionality of the component is not influenced by a potential difference to ground of up to ±1,0 V.

3.13.2 Test

If the DUT has several voltage and ground connections for the BN48, the test must be performed individually for each connection point.

In general, the interface dimensioning between two components must be designed for a ground offset of ±1,0 V.

The component is connected as described in Figure 18.

Table 22: Test parameters E48-10 Ground offset

DUT operating mode	Operating mode II.c
V_{48test}	V_{48n}
V_0	1,0 V
Number of cycles	Both switching positions
Number of DUTs	At least 6

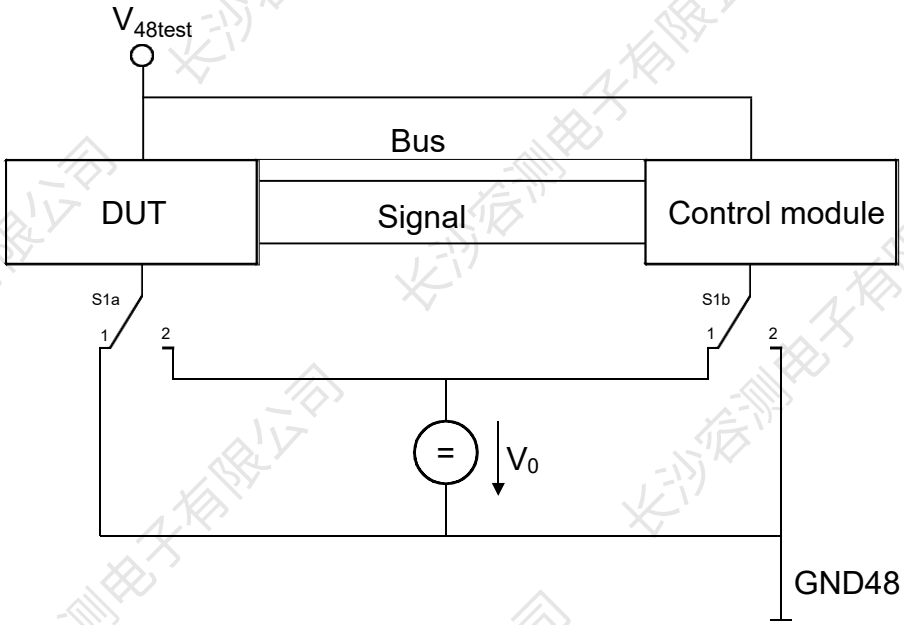

Figure 18: Schematic circuit E48-12 Ground offset (V_{B48})

3.13.3 Requirement

Functional status A

3.14 E48-13 Internal dielectric strength

3.14.1 Aim

The internal dielectric strength between BN48 pins and B12 pins is determined, if both voltages are used in one component.

3.14.2 Test

Table 23: Test parameters E48-13 Internal dielectric strength

DUT operating mode	Operating mode I.a
V_{48test}	$V_{48shprotect}$
t_{test}	60 min
H_{rel}	50%
T_{test}	35 °C
Test points	Application of the test voltage between – both supply connections – other test points agreed upon with the appropriate department Refer to Figure 19
Number of cycles	1
Number of DUTs	6

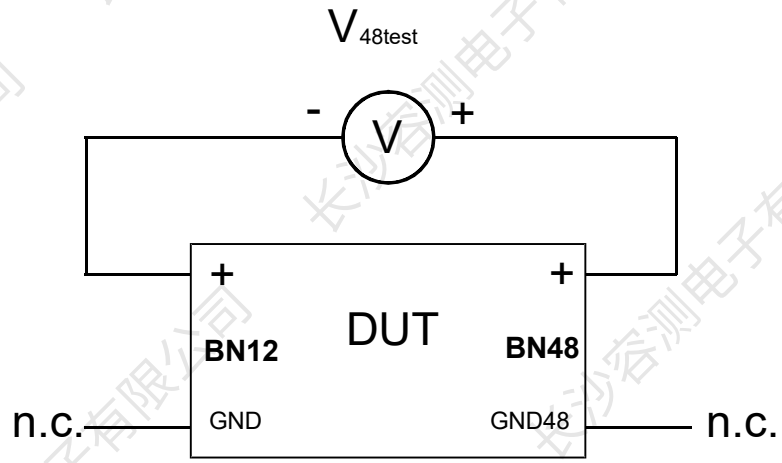

Figure 19: Schematic circuit E48-13 Internal dielectric strength

3.14.3 Requirement

The insulation resistance must be at least 1 MΩ. It must be verified that the DUT has not been damaged.

Functional status A after the test

3.15 E48-14 Closed-circuit current

3.15.1 Aim

The closed-circuit current consumption for closed-circuit relevant components is determined.

3.15.2 Test

For components with post-run function (e.g. fan), the closed-circuit current consumption must be determined after the follow-on current has stopped.

Table 24: Test parameters E48-14 Closed-circuit current

DUT operating mode	Operating mode II.a	
V_{48test}	V_{48n}	
Test condition	Temperature range	Max. closed-circuit current
	T_{min} to 40 °C	0,1 mA
	40 °C to T_{max}	0,2 mA
Number of DUTs	6	

3.15.3 Requirement

The closed-circuit current consumption target for any DUT is 0 mA.

Post-run functions must be released by the department responsible for closed-circuit current management.

3.16 E48-15 Operation in the range without functional limitation

3.16.1 Aim

The operating behavior at the range limits is examined.

3.16.2 Test

Table 25: Test parameters E48-15 Operation in the range without functional limitation

DUT operating mode	Operating mode II.c
V_0	V_{48n}
V_1	$V_{48min,unlimited}$
V_2	$V_{48max,unlimited}$
t_0	100 ms
t_{f1}	1 ms
t_1	1 s
t_r	1 s
t_2	10 s
t_{f2}	1 s
t_3	100 ms
T_{test}	T_{max}, T_{RT}, and T_{min}
Number of cycles	10
Number of DUTs	6

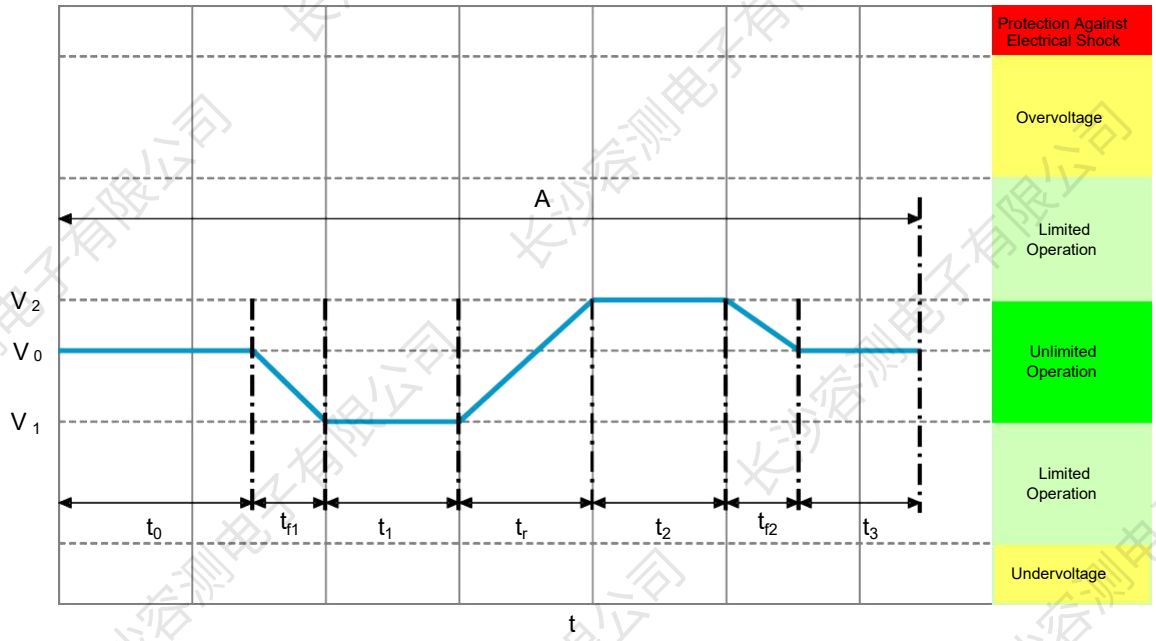

Figure 20: Test pulse E48-15 Operation in the range without functional limitation

3.16.3 Requirement

Functional status A

3.17 E48-16 Operation in the upper range with functional limitation

3.17.1 Aim

The operating behavior during the change and at the range limits is examined.

3.17.2 Test

Table 26: Test parameters E48-16 Operation in the upper range with functional limitation

DUT operating mode	Operating mode II.c
V_0	V_{48n}
V_1	$V_{48max,high,limited}$
V_2	$V_{48max,unlimited}$
V_3	$V_{48max,unlimited}$ + 1 V
t_0	100 ms
t_{r1}	4 s
t_1	10 s
t_{f1}	2 s
t_2	10 s
t_{r2}	2 s
t_3	10 s
t_{f2}	2 s
t_4	100 ms
T_{test}	T_{max}, T_{RT}, and T_{min}
Number of cycles	10
Number of DUTs	6

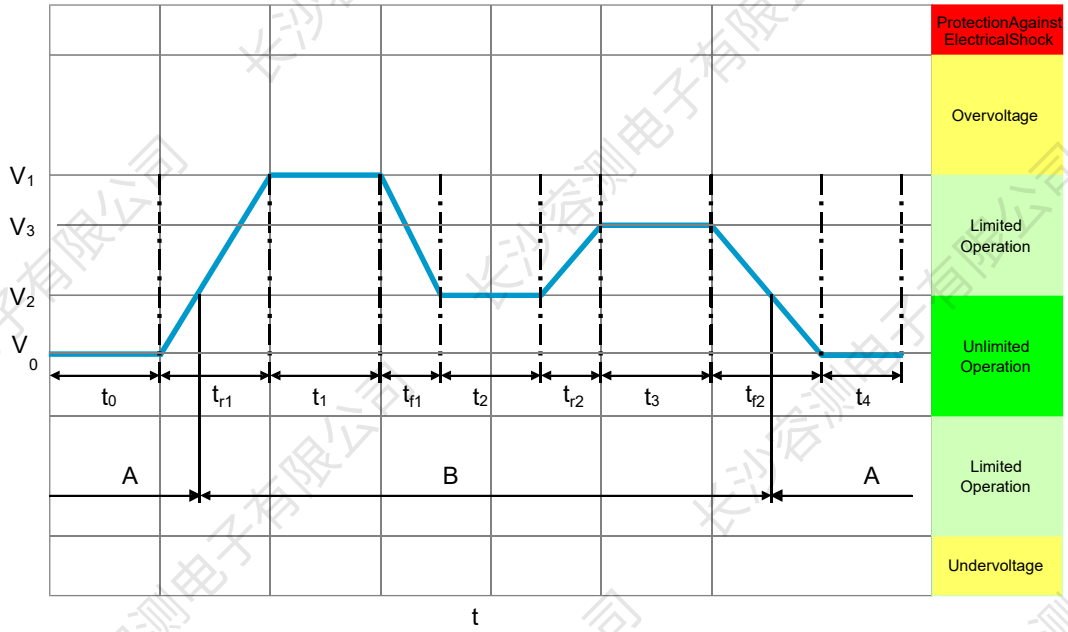

Figure 21: Test pulse E48-16 Operation in the upper range with functional limitation

3.17.3 Requirement

See Figure 21: No error is entered in the event memory.

3.18 E48-17 Operation in the lower range with functional limitation

3.18.1 Aim

The operating behavior during change and at the range limits is examined.

3.18.2 Test

Table 27: Test parameters E48-17 Operation in the lower range with functional limitation

DUT operating mode	Operating mode II.c
V_0	V_{48n}
V_1	$V_{48min,low,limited}$
V_2	$V_{48min,unlimited}$
V_3	$V_{48min,low,limited}$ + 1 V
t_0	100 ms
t_{f1}	2 s
t_1	10 s
t_{r1}	4 s
t_2	10 s
t_{f2}	2 s
t_3	10 s
t_{r2}	2 s
t_4	100 ms
T_{test}	T_{max}, T_{RT}, and T_{min}
Number of cycles	10
Number of DUTs	6

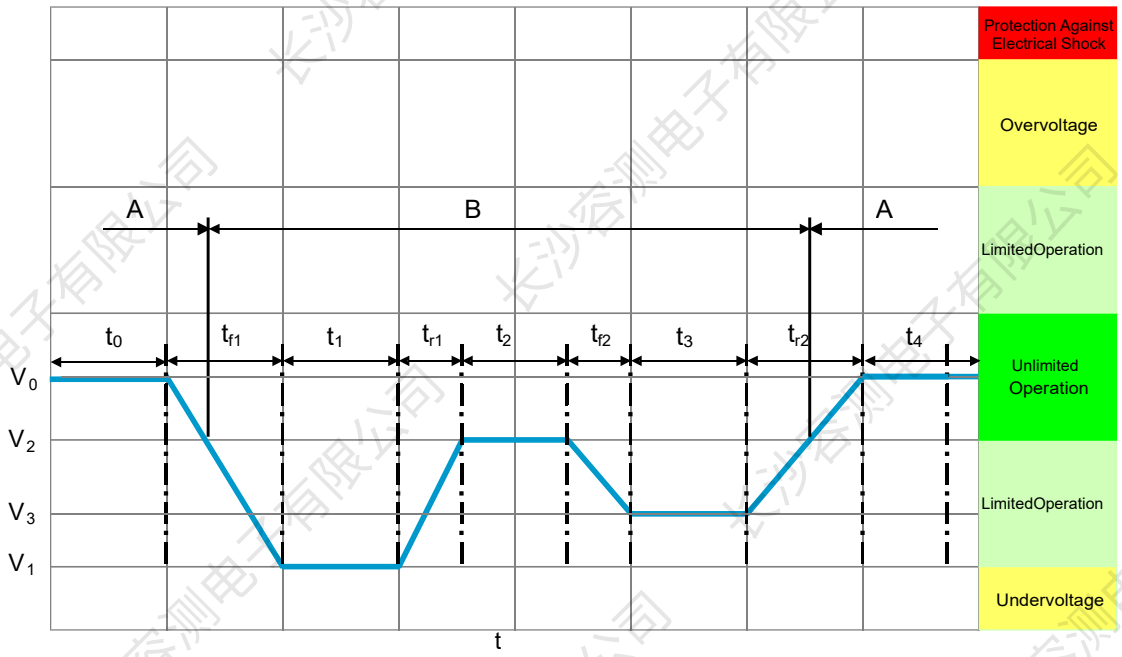

Figure 22: Test pulse E48-17 Operation in the lower range with functional limitation

3.18.3 Requirement

See Figure 22: No error is entered in the event memory.

3.19 E48-18 Overvoltage range

This test is used to simulate the load switch-off during storage charging and examine the changes in operational behavior up to the overvoltage range.

3.19.1 Test

Table 28: Test parameters E48-18 Overvoltage range

DUT operating mode	Operating mode II.c
V_0	V_{48n}
V_1	V_{48r}
V_2	$V_{48max,unlimited}$ + 1 V
t_0	100 ms
t_{r1}	10 ms
t_1	1 s
t_{f1}	1 s
t_2	10 s
t_{r2}	1 ms
t_3	2 s
t_{f2}	1 s
t_4	5 s
t_{r3}	10 s
t_5	2 s
t_{f3}	10 s
t_6	100 ms
T_{test}	T_{max}, T_{RT}, and T_{min}
Number of cycles	10
Number of DUTs	6

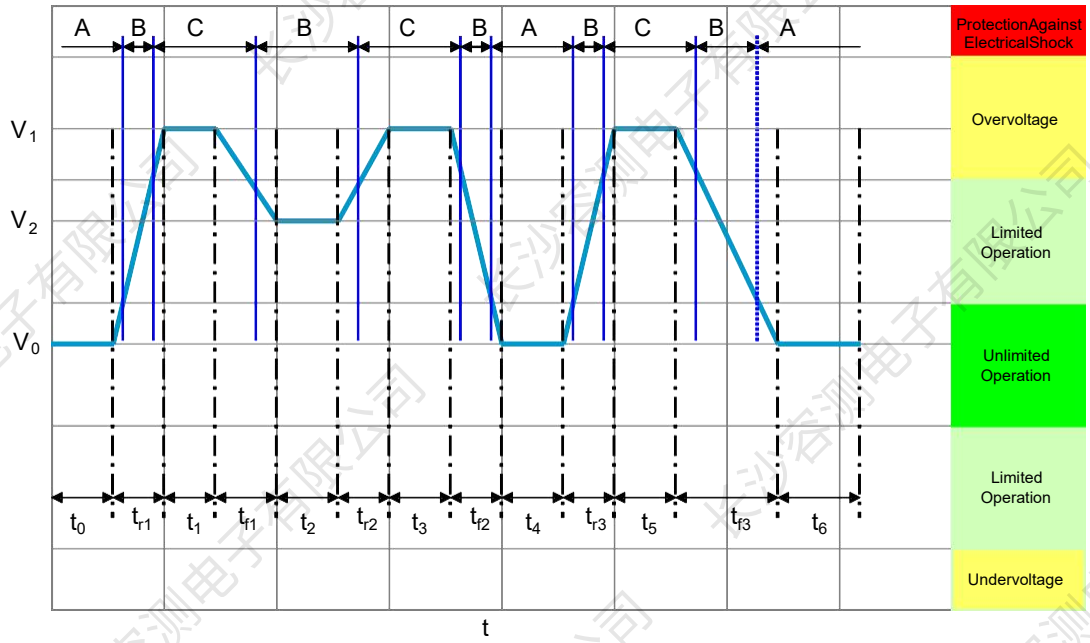

Figure 23: Test pulse E48-18 Overvoltage range

3.19.2 Requirements

See Figure 23: Test pulse E48-18 Overvoltage range.
Only the error overvoltage must be entered in the event memory.

3.20 E48-19 Undervoltage range

3.20.1 Aim

The changes in operational behavior up to the undervoltage range are examined.

3.20.2 Test

Table 29: Test parameters E48-19 Undervoltage range

DUT operating mode	Operating mode II.c
V_0	V_{48n}
V_1	$V_{48stoprotect}$
V_2	$V_{48min,low,limited}$ + 6 V
t_0	100 ms
t_{f1}	1 s
t_1	1 s
t_{r1}	10 ms
t_2	10 s
t_{f2}	1 s
t_3	2 s
t_{r2}	1 ms
t_4	5 s
t_{f3}	10 s
t_5	2 s
t_{r3}	10 s
t_6	100 ms
T_{test}	T_{max}, T_{RT}, and T_{min}
Number of cycles	10
Number of DUTs	6

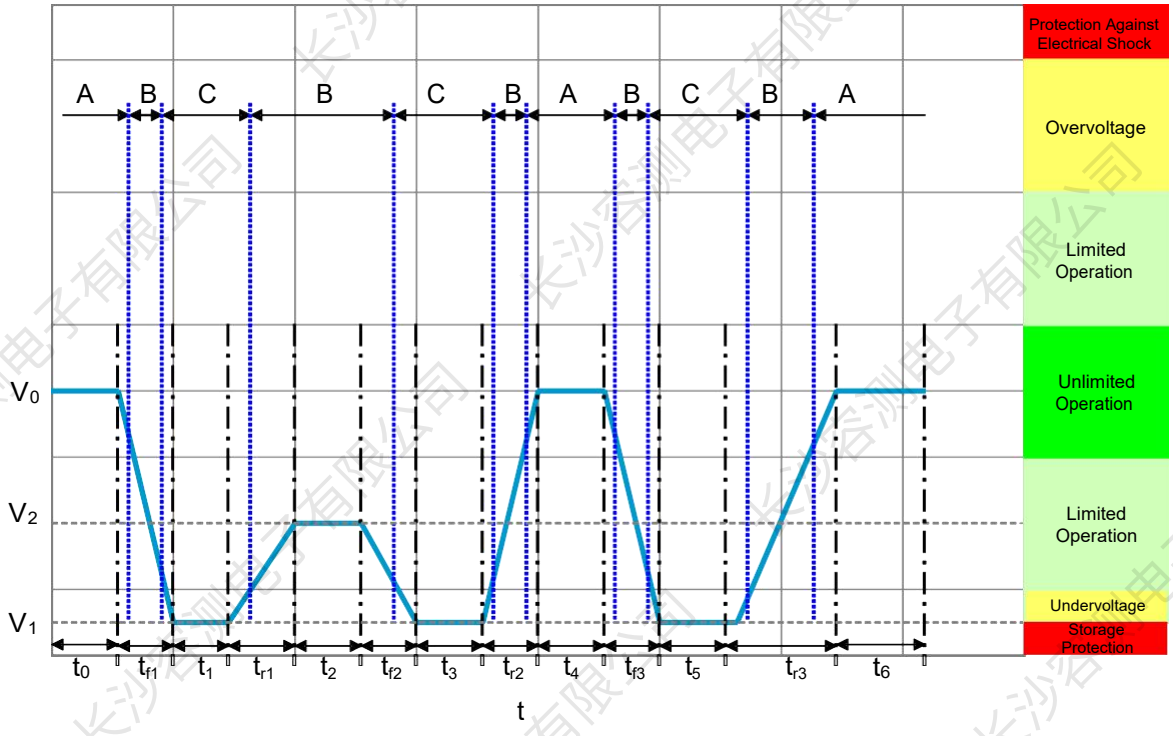

Figure 24: Test pulse E48-19 Undervoltage range

3.20.3 Requirement

See Figure 24: Test pulse E48-19 Undervoltage range.
Only the error undervoltage must be entered in the event memory.

3.21 E48-20 Fault current, part 1

3.21.1 Aim

The fault current resistance of a component with connection to both electric systems (BN12 and BN48) is examined.

3.21.2 Test

The DUT is connected on a test bed as per Figure 25: Schematic circuit E48-20 Fault current, part 1.

Switch S1 is open (T.41 is disconnected).

T.40 is supplied (the behavior at two different voltages is tested).

The BN12 part of the component is supplied.

The current must be measured that flows through the component's T.40.

Table 30: Test parameters E48-20 Fault current, part 1

DUT operating mode	II.a
Test setup	Refer to Figure 25
V_{48test}	a) V_{48n}
	b) $V_{48shprotect}$
V_{12test}	14 V
t_{test}	10 min
T_{test}	T_{RT}
Number of cycles	1
Number of DUTs	6

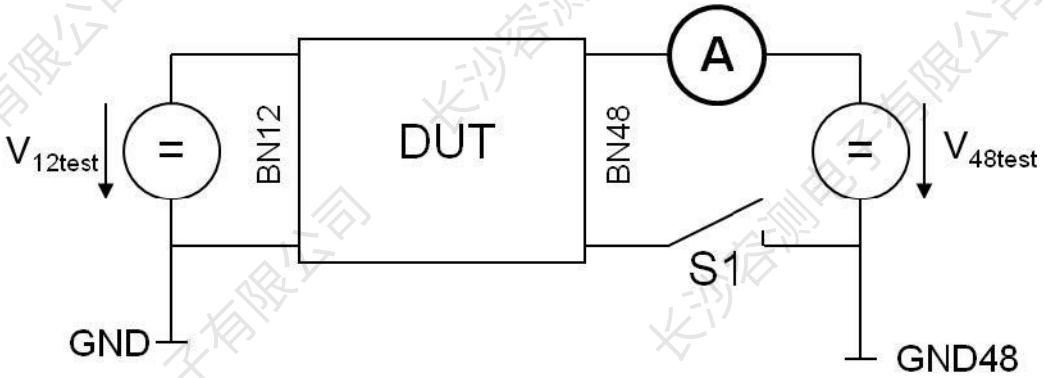

Figure 25: Schematic circuit E48-20 Fault current, part 1

3.21.3 Requirement

The following applies to the T.40 supply current:

$|I| \leq 1\ \mu A$

3.22 E48-20 Fault current, part 2

3.22.1 Aim

The fault current resistance of a component with connection to both electric systems (BN12 and BN48) is examined.

3.22.2 Test

The DUT is connected on a test bed as per Figure 26: Schematic circuit E48-20 Fault current, part 2.

Switches S1, S2, S3, and S4 are open (the DUT is not supplied).

All BN12 contacts (supply and communication) are connected to each other (short-circuited).

All BN48 contacts (supply) are connected to each other (short-circuited).

0 V is applied to both BN12 and BN48. A test voltage of 70,0 V is applied between BN48 and BN12.

The current must be measured that flows through this 70-V supply and therefore through the component.

Table 31: Test parameters E48-20 Fault current, part 2

Test setup	Refer to Figure 26
V_{48test}	V_{48n}
V_{12test}	14 V
t_{test}	10 min
T_{test}	T_{RT}
Number of cycles	1
Number of DUTs	6

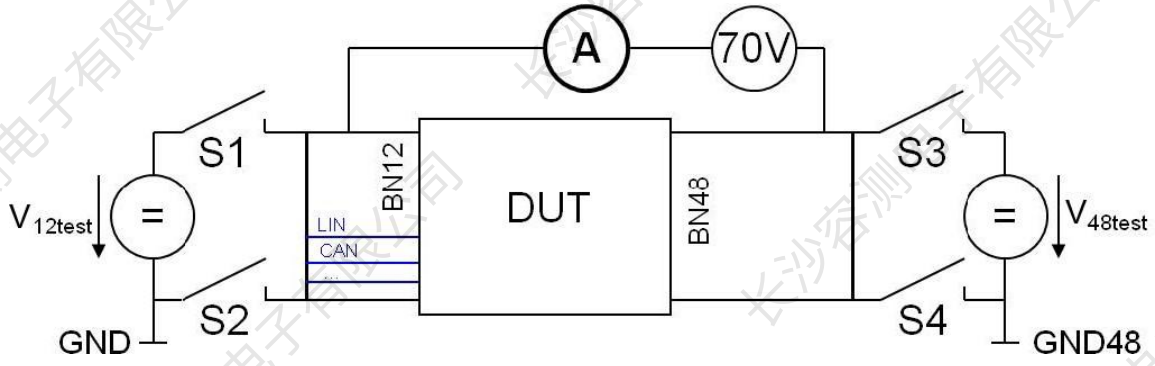

Figure 26: Schematic circuit E48-20 Fault current, part 2

3.22.3 Requirement

The following applies to the current between BN12 and BN48:

$|I| \leq 1\ \mu A$

3.23 E48-21 Short circuit in signal circuit and load circuit

3.23.1 Aim

Short circuits on all BN48 device inputs and outputs and in the BN48 load circuit are examined. All BN48 in- and outputs must be designed to be short-circuit resistant against the test voltage and GND48. The following tests must be conducted:

- with activated and not activated outputs
- without voltage supply
- without ground

3.23.2 Test

Table 32: Test parameters E48-21 Short circuit in signal circuit and load circuit

DUT operating mode	Operating mode II.c
Test duration	Each BN48 pin is short-circuited for 60 s, once to test voltage and once to GND48
Test voltage	$V_{48max,unlimited}$ and $V_{48min,unlimited}$
Test setup	The power supply unit used for the test must be able to supply the short-circuit currents to be expected by the component.
Number of cycles	Each pin, once to test voltage and once to GND48
Number of DUTs	6

3.23.3 Requirement

To pass the test, the following functional statuses must be achieved:

- For inputs and outputs (I and O): functional status C
- For supply voltages (PWR): functional status D
- For device ground (GND48): functional status D

Glossary and abbreviations

Table 33: Abbreviations

Abbreviation	Definition	Explanation
BN12	12 V vehicle power supply	12 V electric system
BN24	24 V vehicle power supply	24 V electric system
BN48	48 V vehicle power supply	48 V electric system
DUT	Device under test	Device under test
EM	Event memory	Event memory
GND	Ground	Electrical ground
PES	Partial vehicle power supply	Partial electric system
A, B, C, D in diagram	Functional status	Functional statuses A, B, C, D